



PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT (PCT Article 36 and Rule 70)

Applicant's or agent's file reference JL3618	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/PEA416)	
International application No. PCT/GB 03/00971	International filing date (day/month/year) 07.03.2003	Priority date (day/month/year) 16.03.2002
International Patent Classification (IPC) or both national classification and IPC H01Q3/26		
Applicant QINETIQ LIMITED et al.		
<p>1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.</p> <p>2. This REPORT consists of a total of 6 sheets, including this cover sheet.</p> <p><input checked="" type="checkbox"/> This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).</p> <p>These annexes consist of a total of 9 sheets.</p>		
<p>3. This report contains indications relating to the following items:</p> <ul style="list-style-type: none"> I <input checked="" type="checkbox"/> Basis of the opinion II <input type="checkbox"/> Priority III <input type="checkbox"/> Non-establishment of opinion with regard to novelty, inventive step and industrial applicability IV <input type="checkbox"/> Lack of unity of invention V <input checked="" type="checkbox"/> Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement VI <input type="checkbox"/> Certain documents cited VII <input type="checkbox"/> Certain defects in the international application VIII <input type="checkbox"/> Certain observations on the international application 		
Date of submission of the demand 19.09.2003	Date of completion of this report 02.02.2004	
Name and mailing address of the international preliminary examining authority:  European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer von Walter, S-U Telephone No. +49 89 2399-8255 <div style="text-align: right;">  </div>	

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT**

International application No. **PCT/GB 03/00971**

I. Basis of the report

1. With regard to the **elements** of the international application (*Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17)*):

Description, Pages

1-14, 17, 20-25	as originally filed
15, 16, 18, 19	received on 14.01.2004 with letter of 12.01.2004

Claims, Numbers

1-24	received on 14.01.2004 with letter of 12.01.2004
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Drawings, Sheets

1/6-6/6	as originally filed
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2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT**

International application No. PCT/GB 03/00971

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	1-17,20,21
	No: Claims	18,19,22-24
Inventive step (IS)	Yes: Claims	7
	No: Claims	1-6,8-24
Industrial applicability (IA)	Yes: Claims	1-24
	No: Claims	

2. Citations and explanations

see separate sheet

1. Section V:

In this report, reference is made to the following documents:

D1= GB-A-2 188 782

D2= Scott I. et. al.: "A sparse approach in partially adaptive linearly constrained arrays", Acoustics, Speech and Signal Processing, 1994 International Conference on Adelaide, SA, Australia, 19-22 April 1994, pages IV-541 - IV-544, ISBN: 0-7803-1775-0, XP010134087

2. The subject-matter of claim 1 lacks inventive step (Article 33 (3) PCT):

D1 shows a signal processing system having a plurality of input channels (D1, page 3, lines 14-25, D1, Fig. 4, antenna elements); sampling means adapted to obtain a first signal sample from at least a first of the plurality of input channels at a first time and a second signal sample from a second of the plurality of input channels at a second time (D1, page 3, lines 14-31, D1, Fig. 4, A-D converters); switching means for switching said sampling means between input channels (D1, page 3, lines 29-31, D1, Fig. 4, multiplexer); and processing means for processing said signal samples, the processing means being arranged to generate an output suitable for sending to beamforming means, said output being related to at least one weighting coefficient associated with at least one of said input channels and being generated using an iteration of an error minimisation routine executed by the processing means using said first signal sample to cause a first output at a first time and using said second signal sample to cause a second output at a second time, the sampling means being arranged to sample each input channel in a predetermined order (D1, page 3, lines 14-31, D1, Fig. 4, LMS processor operating in a time-multiplexed manner).

Consequently, the subject-matter of claim 1 differs from what is disclosed in D1 only in that

- a. the processing means is arranged to determine an input channel which makes a significant contribution to a gradient of an error function and to use a signal from

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT - SEPARATE SHEET**

International application No. PCT/GB03/00971

- said channel in the error minimisation routine (feature a) and
- b. the sampling means comprise fewer analogue to digital converters, intermediate the switching means and the processing means, than there are input channels (feature b).

However, as to

feature a,
iteratively determining input data out of a subset of a plurality of input data which best minimizes an error function is a known strategy for solving the problem of reducing complexity of an iterative algorithm (c.f. D2, page IV-543, paragr. "A sparse approach"). Therefore, using this strategy for updating the weighting vector and weighting error in the procedure shown in D1, page 5, line 25 - page 6, line 54 is obvious; and

feature b,
using a reduced number of analogue to digital converters due to the reduced number of inputs to the processor is an obvious design procedure to further reduce the complexity of the system (cf. D1, page 6, lines 47-48).

Therefore, features a and b are not adapted to lend inventive step to claim 1.

3. The subject-matter of dependent claims 2-6 and 8 are known from D1 (claims 3 and 5) and D2 (claims 2 and 8) or refer to modifications not presenting an unexpected effect. These claims are not inventive, Article 33(3) PCT.
4. The considerations of items 2 and 3 above apply equally to corresponding method claims 9-14 and claims 15-17.
5. The subject-matter of claim 18 is not new (Article 33 (2) PCT):

**INTERNATIONAL PRELIMINARY
EXAMINATION REPORT - SEPARATE SHEET**

International application No. PCT/GB03/00971

D1 shows an adaptive filter having
a plurality of input channels (D1, Fig 4, antenna elements),
a switch (D1, Fig. 4, multiplexer) and
a processor (D1, Fig. 4, LMS processor).

The switch is arranged to switch a subset of said input channels in and out of operative communication with the processor such that said processor processes signals from different channels at different times (D1, page 3, lines 14-31, D1, page 6, lines 42-54).

Hence, D1 discloses a filter having all features present in claim 18.

6. Claims 19 and 22-24 do not present subject-matter which goes beyond the filter described in D1, page 3, lines 14-31 and D1, Fig. 4. These claims are equally not new (Article 33 (2) PCT).
7. Claims 20 and 21 lack inventive step, and reference is made to item 2 above (Article 33 (3) PCT).
8. The subject-matter of claim 7 is not known nor rendered obvious by the available prior art and considered to meet the requirements of Article 33 (2) and (3) PCT.

Figure 9 is a schematic representation of a WLAN having an access point including a phased array antenna according to at least one aspect of the present invention.

5 Referring now to Figure 1, a phased array antenna 100 employing a conventional least means squared (LMS) architecture comprises a plurality of receiving elements 102a-n each having a respective weighting unit 104a-n associated therewith, a summation unit 106 and control electronics 108. Typically the number of receiving elements in an array
10 varies with the desired degree of accuracy of the systems. This is because the more elements present in an array the higher the number of degrees of freedom of the systems.

The summation unit has an output 112 that is the summation of all the
15 beamformed input signals from the receiving elements 102a-n. The control electronics 108 comprises a comparator 114, a processor 115, sampling devices 116a-n, typically an inductive coupling device, and analogue to digital converters (ADC) 117a-n.

20 The comparator 114 has first and second inputs 118, 120 and an output 122. The first input 118 receives a portion of the signal, $y(n)$, from the output 112. The second input 120 receives a training signal, $d(n)$, that should, if the weights applied by the weighting units 104a-n are correct, correspond to the expected output from the summation unit. The
25 comparator 114 generates an error function signal, $e(n)$, based upon the difference between the output signal $y(n)$ and the training signal $d(n)$ that is output to the processor 115 via the output 122.

Each of the receiving elements 102a-n is sampled by its respective
30 sampling device 116a-n. The sampled analogue signal is digitised using a respective one of the plurality of ADC's 117a-n and passed to the

processor 115. Each channel 102a-n having an associated ADC 117 a-n results in both the cost and the power consumption of the prior art arrangement increasing over that of a system according to the present invention.

5

The processor 115 reduces the error functions, $e(n)$, by iteratively applying the following vector least means squared algorithm in n -dimensions, where n is the number of receiving elements 102a-n:

$$\underline{w}_{k+1} = \underline{w}_k + \mu \varepsilon' \underline{x}_n$$

10

This algorithm reduces the error function signal, $e(n)$, between the signal output from the summation unit and the training signal by varying the complex weighting functions applied to the weighting units 104a-n in order to vary the output signal from the summation unit such that the error surface formed by the error function, $e(n)$, is descended in the direction of maximum gradient. An estimate of the gradient vector at each iteration is obtained from the product of the error signal and a 'snapshot' of each of the vector of signals received at the receiving elements 102a-n. The convergence time of the algorithm is sufficiently short that a near zero error signal is achieved, subject to random signal noise, before the coherence time, i.e. the length of time for which the training signal is valid, of the training signal is exceeded.

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Referring now to Figure 2, an n -dimensional error surface 200 is constructed of n vectors 202a,b (only 2 shown) and is generally quadratic in form. In a full LMS analysis the phase and amplitude of each of these vectors must be compared with respective signals from the input channels 102a-n simultaneously in order to move towards a minimum 204 of the error surface 200.

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excluded from a channel is determined by the number of degrees of freedom of the sensor array. For a sensor array having n elements there are $n-1$ degrees of freedom that can be nulled.

5 Referring now to Figure 4, a signal coupling arrangement 400, such as may be used in sampling devices 116, comprises a local oscillator (LO) 402, a coupling region 404, a signal pick up 405, an amplifier 406, an ADC 408. The ADC 408 includes a sample-and-hold circuit 410, an ADC unit 412 and a clock input 414.

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A signal passes from the LO 402 to the coupling region 404 where the pick up 405 is, typically, inductively coupled to the coupling region 404. The coupled signal is then amplified by the amplifier 406 and passes to the ADC 408. The digitised signal is then input to the processor 115 and
15 is processed in order to calculate a complex weighting coefficient for the signal.

The calculated adaptive complex weighting coefficients are passed to the respective weighting units 104a-n.

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The foregoing discusses the prior art.

Referring now to Figure 5, this shows a new phased array antenna 500 that employs a switched LMS architecture and is substantially similar to
25 the phased array antenna 100 of Figure 1, similar parts thereto are accorded the same reference numerals in the five hundred series.

The phased array antenna 500 comprises a plurality of receiving elements 502a-n each having a respective weighting unit 504a-n associated
30 therewith, a summation unit and control electronics.

The summation unit 510 outputs a signal to the control electronics that is the summation of all of the beamformed input signals from the receiving elements 502a-n. The control electronics comprises a comparator 514, a processor 515, and a sampling devices 516a-n, typically an inductive
5 coupling device.

The weighted signals pass to a summation unit 510 from where a summed signal, $y(n)$, is output. A portion of the summed signal is input to a comparator 514, as is a training signal $d(n)$. The training signal is, of
10 course, of known sequence/form. An error function signal $e(n)$ that is the difference between the summed signal $y(n)$ and the training signal $d(n)$ is output to a processor 515.

Each of a plurality of receiving elements 502a-n is sampled by a
15 respective sampling device 516a-n prior to an incoming signal being subjected to complex weighting by respective weighting units 504a-n.

Each of the signals sampled by the sampling device 516a-n passes along a respective data channel 525a-n to a switching unit 527. The switching
20 unit 527 contains a switch 529, typically a solid state switch, an ADC 533 and a plurality of switch contacts 535a-n corresponding to the ends of the data channels 525a-n. Of course, mechanical or other switches could be used instead of a solid state switch.

25 Within the switching unit 527 a single switch contact 535a is closed with the switch 529 corresponding to a single receiving element 502 at each iteration of an LMS algorithm. The processor 515 makes an estimate of the component of the error vector at each iteration and a single complex weight of the weight vector corresponding to that to be applied to the
30 receiving element 502a is updated.

CLAIMS

1. A signal processing system comprising a plurality of input channels, sampling means adapted to obtain a first signal sample from at least a first of the plurality of input channels at a first time and a second signal sample from a second of the plurality of input channels at a second time, switching means for switching said sampling means between input channels, and processing means for processing said signal samples, the processing means being arranged to generate an output suitable for sending to beamforming means, said output being related to at least one weighting co-efficient associated with at least one of said input channels and being generated using an iteration of an error minimisation routine executed by the processing means using said first signal sample to cause a first output at a first time and using said second signal sample to cause a second output at a second time, the sampling means being arranged to sample each input channel in a predetermined order and the processing means is arranged to determine an input channel which makes a significant contribution to a gradient of an error function and to use a signal from said channel in the error minimisation routine wherein the sampling means comprise fewer analogue to digital converters, intermediate the switching means and the processing means, than there are input channels.
2. A system according to claim 1 wherein an input channel making significant contribution to the gradient of the error function constitutes an input channel, which when ranked by contribution to the gradient of the error function, is within any one of the following top percentiles of the sampled signals: 1%, 5% 10%, 25%, 50%.
3. A system according to either of claims 1 or 2 wherein the sampling means include at least one ADC.

4. A system according to any preceding claim wherein there are provided a maximum of four sampling means.
- 5 5. A system according to any preceding claim wherein the switching means is arranged to switch between input channels either in a predetermined order or randomly.
6. A system according to any preceding claim wherein there are
10 provided a maximum of half the number of sampling means as there are input channels.
7. A system according to any preceding claim wherein the sampling means is arranged to sample the at least one input channel at the end of a
15 symbol period.
8. A system according to any preceding claim wherein the processing means is arranged to determine which input channel has the largest contribution to the gradient of the error function and use the signal from
20 said channel in the error minimisation routine.
9. A method of signal processing comprising the steps of:
- i) sampling a sample signal of a subset of a plurality of input channels;
- 25 ii) digitising said sample using fewer analogue to digital converters than there are input channels, wherein said analogue to digital converters are intermediate the input channels and a digital processing means;
- iii) reducing an error function using said sample, using the digital
30 processing means;

- iv) switching between the subset and another subset of the plurality of input channels using switching means, or resampling the same subset as in step (i); and
- v) determining which of the input channels make significant contributions to a gradient of the error function and switching to a gradient of the error function and switching to said channel prior to step (iii).

10. The method of claim 9 including defining an input channel making significant contribution to the gradient of the error function constitutes an input channel, which when ranked by contribution to the gradient of the error function, is within any one of the following top percentiles of the sampled signals: 1%, 5%, 10%, 25%, 50%.

11. The method of either of claims 9 or 10 including repeating steps (i) to (iv), iteratively, in order to obtain a minima in the error function.

12. The method of either of claims 9 to 11 including generating at least one weighting coefficient associated with the subset of input channels based upon the result of the reduction of the error function.

13. The method of any one of claims 9 to 12 including switching between the subsets of channels between that are selected either in a predetermined order or randomly at step (iv).

14. The method of any one of claims 9 to 13 including determining, at step (v), which of the input channels makes the largest contribution to a gradient of the error function and switching to said channel prior to step (iv).

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15. A telecommunications system including a signal processing system according to any one of claims 1 to 8 wherein the telecommunications system is a WLAN.
- 5 16. A system according to claim 15 wherein the signal processing system is an access point that is arranged to spatially null a network element from a piconet.
- 10 17. A method of increasing the number of users that can access a telecommunications channel of a given bandwidth incorporating the method of any one of claims 9 to 14.
- 15 18. An adaptive filter comprising a plurality of input channels, a switch, a processor, said switch being arranged to switch a subset of said input channels in and out of operative communication with the processor such that said processor processes sample signals from different channels at different times.
- 20 19. A filter as claimed in claim 18 wherein the processor is arranged to process said sample signals so as to create respective adaptive profile of weighting coefficients for each respective of said input channels.
- 25 20. A filter as claimed in either of claims 18 or 19 wherein there is provided an ADC intermediate said switch and said processor.
21. A filter according to any one of claims 18 to 20 wherein the switch is arranged to switch which input channels are connected to the ADC.
- 30 22. A method of adaptive filtering comprising obtaining a sample signal, or signals, from a plurality of channels and using the sample signals to form at least one weighting coefficient for at least one of the

channels, the weighting coefficients being obtained by performing an error function reduction iteration associated with the difference between the sampled signal, or signals, and a reference values, the error function being reduced by operating on a sample signal, or signals, from a subset
5 of the available channels that is smaller than the number of available channels, and changing the channel, or channels, present in the subset between at least two iterations of the reduction of the error function.

23. The method of claim 22 including providing switching means to
10 switch between subsets of channels.

24. The method of either of claims 22 or 23 including providing a subset of channels that is significantly smaller than the total number of channels.

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